REMARKS/ARGUMENT

Applicants submit herewith a new oath that acknowledges the filing of the foreign application, as requested by the Examiner.

The Examiner has determined that the title of the invention is not descriptive. By this amendment the title has been amended from "WRITE BACK POLICY FOR MEMORY" to instead be --WRITE BACK POLICY FOR MEMORY BASED ON STACK TREND INFORMATION--. Applicants believe this to be more descriptive of their invention that the title suggested by the Examiner.

Applicants' acknowledge the Examiner's objection to the disclosure. By this amendment, paragraphs 0001, 0019, 0021 and 0023 have been amended to conform to the Examiner's recommendations. As such, the objections are overcome.

Claims 13, 14 and 20 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejections.

Applicants traverse the Examiner determination that there is a conflict between "decoder" and "decode logic" in Claim 12 since "decode logic" is not found in Claim 12. Applicants similarly traverse the Examiner's determination that line 1 of Claim 15 recites the term "the cache memory". Reference to Claim 15 clearly discloses a recitation of "a cache memory". Accordingly, there is no antecedent basis issue.

1) Claims 1-4, 8, 11 and 13 stand rejected under 35 U.S.C. 102(b) as being unpatentable over Shen et al. (U.S. Patent 5,687,336) (hereinafter "Shen"). Applicants respectfully traverse this rejection as set forth below.

In order that the rejection of Claims 1-4, 8, 11 and 13 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites, a method of managing memory, comprising: "**examining** current and future instructions operating on a stack", "**determining stack trend information**" and "utilizing **the trend information to reduce data traffic between various levels of a memory**".

Independent Claim 11 as amended, requires and positively recites, a computer system, comprising: "a processor; a memory coupled to the processor", "a stack that exists in memory and contains stack data", "a memory controller coupled to the memory", "**trend logic**", "wherein the processor executes instructions", "wherein the **trend logic provides trend information about the stack to the controller**" and "wherein the **trend information about the stack is based on at least one future instruction**".

In contrast, Shen discloses a pipelined processor that executes several stack instructions simultaneously (Abstract, lines 1-2). The stack-top address is generated early in the pipeline. Other stack instruction in the pipeline **which have not yet incremented the**

stack pointer are located with a stack valid bit array (Abstract, lines 7-9). The stack valid array **indicates the increment or decrement amounts for stack instructions in each pipeline stage** (Abstract, lines 9-11). An **overall displacement or increment value is computed as the sum of all increments and decrements for stack instruction in the pipeline which have not yet updated the stack pointer** (Abstract, lines 11-14). The overall displacement which accounts for all unfinished stack instruction is added to the stack pointer from the register file to generate the stack-top address (Abstract, lines 15-17). Thus the new stack pointer does not have to be generated before the stack memory is accessed (Abstract, lines 17-19).

There is no teaching in Shen (col. 3, line 65, col. 7, line 7 and Fig. 2) for "examining" current and future instructions operating on a stack, as suggested by the Examiner. Even though Shen discloses on col. 3, line 65, a five-stage pipeline, it says nothing about **examining** current and future instructions operating on a stack. Similarly, while col. 7, line 7 teaches that the stack valid bits for all three pipelines are set to zero, again, it says nothing about **examining** current and future instructions operating on a stack. Further, there is nothing in Fig. 2 that teaches or suggest, **examining** current and future instructions operating on a stack. As such, Shen fails to teach or suggest, "**examining** current and future instructions operating on a stack", as required by Claim 1.

Similarly, there is no teaching in Shen (col. 4, lines 11-15 and 36-60; and Fig. 2) for **determining stack trend information**, as suggested by the Examiner. Shen discloses on col. 4, lines 11-15 that an instruction is first decoded in the D stage instruction decoder 16 and fields in the instruction can indicate which register in register file 10 are accessed by the instruction. This teaching says nothing, however, about "determining stack trend information", as suggested by the Examiner. Similarly, lines 36-60 fail to teach or suggest, **determining stack trend information**, as suggested by the Examiner. Even if, arguendo, stack pointer indicates a higher number or lower

number for its final value, such number is a number - not a TREND or TREND INFORMATION. As such, Shen fails to teach or suggest, "**determining stack trend information**", as required by Claim 1 OR "**trend logic**", as required by Claim 11.

Further, even were there to be a determination of trend information in Shen, which there is not, there is no additional teaching that such information is used to reduce traffic between various levels of a memory, as suggested by the Examiner. Col. 2, lines 23-27 sets forth nothing more than a desire on the part of Shen to develop a pipelined processor for executing multiple stack instructions being simultaneously executed in various stages of the pipeline **without adding many extra stack registers and busses for the stack pointer**. There is no teaching or suggestion for utilizing "trend information" to "reduce data traffic between various levels of a memory". As such, Shen fails to teach or suggest, "utilizing **the trend information to reduce data traffic between various levels of a memory**", as required by Claim 1 OR "wherein the **trend information about the stack is based on at least one future instruction**", as required by Claim 11. Accordingly, the 35 U.S.C. 102(b) rejection of Claims 1 and 11 over Shen are improper and must be withdrawn.

Claims 2-4 and 8 stand allowable as depending directly, or indirectly, from allowable Claim 1. Claim 13 stands allowable as depending indirectly from allowable Claim 11.

Claim 2 further defines the method of claim 1, wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information", it similarly fails to further teach or suggest, trend information that "includes examining future instructions to determine if the

size of the stack is going to decrease as a result of future instructions". There is no support in the locations in Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; and Fig. 2) that anticipate the additional elements of Claim 2. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 2 over Shen is improper and must be withdrawn.

Claim 3 further defines the method of claim 2, wherein a predetermined number of instructions are used in determining stack trend information. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information" that "includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions", it does NOT further teach or suggest, "wherein a predetermined number of instructions are used in determining stack trend information". There is no support in the locations in Shen cited by the Examiner (col. 3, lines 65-67 and col. 6, lines 47-48) that anticipate the additional elements of Claim 3. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 3 over Shen is improper and must be withdrawn.

Claim 4 further defines the method of claim 3, wherein the number of predetermined instructions is at least two. Claim 4 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information" that "includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions", "wherein a predetermined number of instructions are used in determining stack trend information", it does NOT further teach or suggest, "wherein the

number of predetermined instructions is at least two". There is no support in the locations in Shen cited by the Examiner (col. 3, lines 65-67 and col. 6, lines 47-48) that anticipate the additional elements of Claim 4. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 4 over Shen is improper and must be withdrawn.

Claim 8 further defines the method of claim 1, wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information", it similarly fails to further teach or suggest, "wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions". There is no support in the locations in Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; and Fig. 2) that anticipate the additional elements of Claim 8. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 8 over Shen is improper and must be withdrawn.

Claim 13 further defines the computer system of claim 12, wherein the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decoder. Claim 13 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Further, since Shen does not teach or suggest "trend logic", "wherein the processor executes instructions", "wherein the trend logic provides trend information about the stack to the controller" and "wherein the trend information about the stack is based on at least one future instruction", as required by Claim 11, it similarly fails to further teach or suggest, trend information that "wherein the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decoder". There is no support in the locations in

Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15; col. 4, lines 11-15; col. 4, lines 36-60; and Fig. 2) that anticipate the additional elements of Claim 13. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 13 over Shen is improper and must be withdrawn.

2) Claim 18 stands rejected under 35 U.S.C. 102(b) as being unpatentable over Steely et al. (U.S. Patent 6,801,986) (hereinafter "Steely"). Applicants respectfully submit that this rejection is improper. In order that the rejection of Claim 18 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim". Claim 18 depends from Claim 17. The Examiner readily admits on page 8, lines 5-7 that Steely "does not disclose the exact size of a cache line". The Examiner further admits on page 12, lines 8-12 "Steely does not disclose the exact size of a cache line" and "Steely does not disclose expressly a method, comprising: determining whether the size of a stack is increasing or decreasing." As such, Steely does not teach or suggest, and the Examiner has agreed that Steely does not teach or suggest, all of the elements of Claim 18. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 18 is improper and must be withdrawn.

3) Claim 5 is rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of Ebrahim et al. (U.S. Patent 5,893,121). Applicants traverse this rejection for the reasons set forth below.

Claim 5 further defines the method of claim 3, wherein the cache memory maintains a single dirty cache line for stack data. Claim 5 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, the Examiner admits that, "Shen does not disclose that the cache memory maintains a single dirty cache line for stack data" (Office Action, page 8, paragraph 31). The Examiner relies upon Ebrahim to provide this teaching. Assuming, arguendo, that the Examiner is correct concerning the teaching of Ebrahim, the reference still fails to provide the previously described deficiencies of Shen as related to Claims 1, 2 and 3.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 5 is patentable under 35 U.S.C. § 103(a) over Shen in view of Ebrahim.

4) Claims 6 and 10 are rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of Steely. Applicants traverse this rejection for the reasons set forth below.

Claim 6 further defines the method of claim 3, wherein if a dirty cache line needs to be written back, **then analyzing the trend information**, which includes **determining which word of the dirty cache line is going to be written to.**

Claim 6 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, the Examiner admits that, "Shen does not disclose expressly determining which word of the dirty cache line is going to be written to" (Office Action, page 9, paragraph 33, lines 2-3). The Examiner relies upon Steely to provide this teaching. Assuming, arguendo, that the Examiner is correct concerning the teaching of Steely, the reference still fails to provide the previously described deficiencies of Shen as related to Claims 1, 2 and 3.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 6 is patentable under 35 U.S.C. § 103(a) over Shen in view of Steely.

Claim 10 further defines the method of claim 9, wherein the dirty cache line is written from a cache memory to a main memory. Claim 10 is allowable for the same reasons set forth in support of the allowance of Claim 8. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Even if, arguendo, Steely were to disclose that the dirty cache line is written from a cache memory to a main memory, Steely fails to teach the previously described deficiencies of the Shen reference as reflected in Claims 1, 8 and 9.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, Claim 10 is patentable under 35 U.S.C. § 103(a) over Shen in view of Steely.

5) Claims 12 and 14 are rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of O'Connor et al. (U.S. Patent 6,026,485). Applicants traverse this rejection for the reasons set forth below.

Claim 12 further defines the computer system of claim 11, further comprising an instruction decoder **comprising a first portion that decodes current instructions and a second portion that decodes future instructions.**

Claim 14 further defines the computer system of claim 12, wherein the **second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two.**

Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Further, the Examiner admits that, "Shen does not disclose an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions" (Office Action, page 10, paragraph 36, lines 2-4). The Examiner relies upon O'Connor to provide this teaching. Assuming, arguendo, that the Examiner is correct concerning the teaching of O'Connor, the

reference still fails to provide the previously described deficiencies of Shen as related to Claim 11.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 12 is patentable under 35 U.S.C. § 103(a) over Shen in view of O'Connor.

Claim 14 further defines the method of Claim 12, wherein the second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two. Claim 14 is allowable for the same reasons set forth in support of the allowance of Claim 12. Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Moreover, even if, arguendo, O'Connor were to disclose an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions, O'Connor fails to teach the previously described deficiencies of the Shen reference as reflected in Claims 11 and 12.

6) Claims 17 and 19-20 are rejected under 35 U.S.C. § 103(a) as being obvious over Steely et al. in view of Shen et al. Applicants traverse this rejection for the reasons set forth below.

Independent Claim 17 requires and positively recites, a method, comprising: "issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines", "determining whether the write request refers to a predetermined word within a dirty cache line; and **determining whether the size of a stack is increasing or decreasing**".

The Examiner admits that Steely does not disclose the size of a cache line (Office Action, page 12, lines 9-10). The Examiner further admits that Steely does not disclose "determining whether the size of a stack is increasing or decreasing" (Office Action, page 12, line 13). The Examiner relies upon Shen as providing this teaching.

Shen discloses a pipelined processor that executes several stack instructions simultaneously (Abstract, lines 1-2). The stack-top address is generated early in the pipeline. Other stack instruction in the pipeline **which have not yet incremented the stack pointer** are located with a stack valid bit array (Abstract, lines 7-9). The stack valid array **indicates the increment or decrement amounts for stack instructions in each pipeline stage** (Abstract, lines 9-11). An **overall displacement or increment value is computed as the sum of all increments and decrements for stack instruction in the pipeline which have not yet updated the stack pointer** (Abstract, lines 11-14). The overall displacement which accounts for all unfinished stack instruction is added to the stack pointer from the register file to generate the stack-top address (Abstract, lines 15-17). Thus the new stack pointer does not have to be generated before the stack memory is accessed (Abstract, lines 17-19).

There is no teaching in Shen (col. 3, line 65 - col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; and Fig. 2) for "**determining whether the size of a stack is increasing or decreasing**", as required by Claim 17, as suggested by the Examiner. Even though Shen discloses on col. 3, line 65, a five-stage pipeline, it says nothing about

determining whether the size of a stack is increasing or decreasing. Similarly, while col. 7, line 7 teaches that the stack valid bits for all three pipelines are set to zero, again, it says nothing about **determining whether the size of a stack is increasing or decreasing**. Further, there is nothing in Fig. 2 that teaches or suggest, **determining whether the size of a stack is increasing or decreasing**". As such, any combination of Steely and Shen fails to teach or suggest, "**determining whether the size of a stack is increasing or decreasing**", as required by Claim 17.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 17 is patentable under 35 U.S.C. § 103(a) over Steely in view of Shen.

Claims 19 and 20 stand allowable as depending directly, or indirectly, from allowable Claim 17.

Claim 19 further defines the method of claim 18, wherein the **stack size is increasing and the dirty cache line is written to a main memory**.

Claim 20 further defines the method of claim 18, wherein the **stack size is decreasing and the dirty cache line is retained in the cache memory**.

The Examiner admits that Steely does not disclose that the stack size is increasing (Office Action, page 13, paragraph 40, line 3). The Examiner relies upon Shen as

disclosing that the stack size is increasing (Office Action, page 12, paragraph 40, line 4). However, neither Shen nor Steely teach or suggest that a dirty cache line is written to a main memory when stack size is increasing, as required by Claim 19. Similarly, neither Shen nor Steely teach or suggest that a dirty cache line is retained in the cache memory when stack size is decreasing, as required by Claim 20.

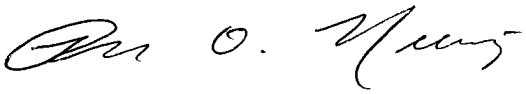
To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claims 19 and 20 are patentable under 35 U.S.C. § 103(a) over Steely in view of Shen.

Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee,* 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Examiner fails to offer ANY rationale for combining Shen with Steely. As such, the Examiner has failed to set forth a prima facie case of the obviousness of Claims 19 and 20. As such, the 35 U.S.C. 103(a) rejection of Claims 19 and 20 is improper and must be withdrawn.

Applicants appreciate the Examiner's determination that Claims 7, 9, 15 and 16 would be allowable if amended to include the limitations of the base claim and any intervening claims. However, Applicants believe Claims 7, 9, 15 and 16 are allowable in their current form for depending from allowable claims. Claims 1-20 are allowable over the cited art. Applicants respectfully requests withdrawal of the rejections and allowance of the application at the earliest possible date. For the record, Applicants note that their amendments to Claims 13, 14 and 20 were purely to overcome an indefiniteness rejection under 35 U.S.C. 112, second paragraph, and not to overcome any prior art.

Respectfully submitted,



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